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The Clarity is in the ASIC ~ Sound Vision delivers an ARM core based platform for next generation karaoke and other consumer electronics.

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Overview and Background

Once Sound Vision decided to create a powerful ASIC platform for consumer electronics, the search for the best architecture was underway. We reviewed all of the solutions available including DSPs and general purpose CPUs. The final choice was ARM for the core and Nucleus for the operating system.

Initially the target market was digital cameras, primarily those with CMOS sensors since we had proprietary image processing algorithms that reduce or eliminate the fixed pattern noise often associated with these devices. We added the ability to record sound so the user could voice-annotate still images, or record short video clips with sound. Sound Vision reference designs for digital cameras were quickly adopted by many major brands including Agfa, Konica, RCA, Polaroid, etc.

Looking to expand the value of the digital camera design, we then added MP3 playback capability with code licensed from ARM. This digital camera plus MP3 player product was subsequently manufactured in Asia by Pretec for Konica.

Venturing further into the audio market, we created a reference design for a karaoke microphone which quickly caught the attention of IVL Technologies, a Canadian firm specializing in digital signal processing for the human voice. They were already supplying professional karaoke systems in Japan with a multi purpose vocal processing unit and wanted to adapt this proprietary technology to a consumer entertainment product, namely, a hand held karaoke microphone, pre-loaded with songs, and ready to plug into the home TV. Their patented system corrects the singer's voice (pitch), generates three part harmony, and can download additional songs over the Internet. IVL also added the ability for the singer to transform their voice to sound like a completely different singer, even of a different gender.

Sound Vision assisted IVL Technologies in porting their unique intellectual property onto the Clarity ASIC and within a few short months, this new device was introduced to rave reviews and widespread commercial success, including "Best Product of 2002" award by USA Today and Business Week magazine. Versions of this technology from IVL are sold by trusted brands such as Bandai and Disney. The newest version includes a video camera that shows the singer on the TV.

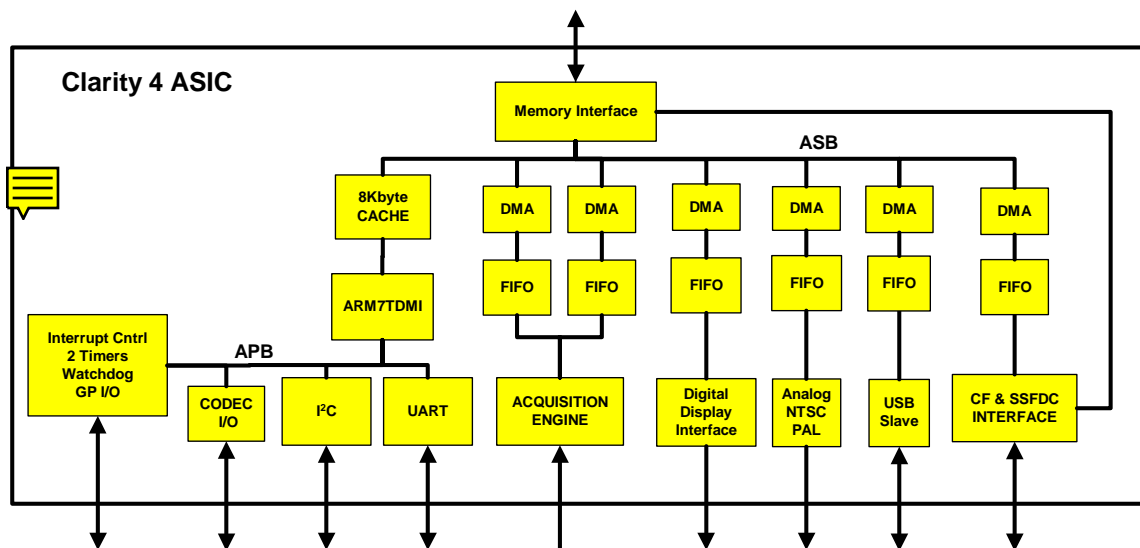
Choosing the Right Architecture

When we began our technical diligence for hardware, we reviewed all of the DSP and CPU solutions offered. We wanted a solution that offered a wide variety of available foundry partners, fast execution of real time tasks, and a rich toolset environment. We chose the ARM solution based upon the following attributes:

- 1) The ARM core was already proven and available from a number of foundries, ensuring a price-competitive setting.

- 2) The single cycle (8 by 16) multiplier in the ARM core was faster in real time multiplies and adds than other available solutions. This is crucial in a device like a digital camera where “dozens” of multiplication and addition operations must be performed on each pixel within a two dimensional array that minimally contains over 300,000 pixels any typically contains more than 1,300,000 pixels.
- 3) ARM offers a robust set of tools for debugging, compiling and linking, plus, it supports multiple programming languages.
- 4) The ARM core is widely endorsed by third party developers with code libraries that include JPEG, MP3, voice recognition, etc. This allows faster time-to-market for new entertainment products such as digital cameras, MP3 players, game systems, TV memory card viewers and karaoke systems.

Chip Architecture



Firmware Description

The Clarity 4 Firmware consists of several main blocks:

- The Nucleus Real Time Operating System
- The Sound Vision Tasks
- The Device Drivers and Interrupt Routines

This firmware typically resides in either NVRAM or ROM on the embedded system board. Parts or all of it are loaded into SDRAM for execution if speed is desired. However, code can be executed from ROM or NVRAM as well.

Choosing the Right Operating System

Our selection criteria for our operating system was that it must be real time, compact enough to run on a minimum of memory, and low cost. We chose the Nucleus RTOS from Accelerated Technology, Embedded Systems Division of Mentor Graphics for the following reasons:

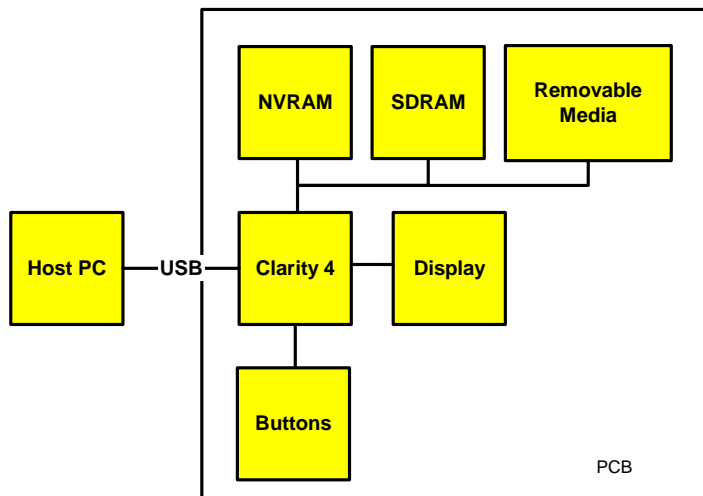
- 1) Nucleus is well suited for a real time multi-tasking application like digital cameras.
- 2) The code is very compact. We run the Nucleus OS plus our own code in typically less than 250 Kbytes of memory.
- 3) The Nucleus source code architecture allows us to write our own interrupt drivers.
- 4) Nucleus is competitively priced and has no run-time royalties
- 5) There is abundant middleware available.

One of the challenges that we faced in our digital camera reference design was picture processing speed, since it is all done in software on the ARM 7. Many of our customers wanted faster "shot to shot" speeds, so that users could take pictures in rapid bursts without having to wait for the previous shot to be processed.

Since the Nucleus RTOS permits multi-tasking, we were able to design the processing task so that it could be interrupted if a second shot was made before the first shot was fully processed and stored as a JPEG file. The subsequent shots have their unprocessed data spooled to SDRAM until it is full, typically a burst of 3 to 5 shots, and then the processing of each image is resumed until the files are stored as JPEGs

Typical System Block Diagram

A typical Clarity 4 based design contains SDRAM as scratch storage, NVRAM for program and data storage, Removable Media for data portability, a display, buttons and a host interface.



Advantages

The principal advantages to building a Clarity based design are:

1. It's an extremely cost effective solution. Clarity is competitively priced, and since it already includes many functions such as NTSC/PAL video out, it helps reduce the total Bill of Materials cost as well. Alternative designs often require several components, each of which may cost as much as Clarity.
2. The combination of the Nucleus OS and the rich assortment of source programs written by Sound Vision and ARM combine to serve as a large base of code that can be a very effective starting point when developing a new product, drastically reducing the time to market.
3. The combination of the USB slave interface and the standard mass storage compliant driver gives a simple way to attach a Clarity based design to a PC or a MAC

Ideal product designs for Clarity are those that require:

1. A display or television interface
2. General purpose programmability.
3. Low cost.

These might include:

1. Cameras
2. Audio Players
3. Programmable Remote controls
4. Karaoke Systems
5. Game Systems
6. TV viewers

As well, Clarity can serve as a replacement for the typical micro-controller in more sophisticated systems, offering the designer a richer graphical interface to a television or other display.

ARM Advantage

Using Clarity 4 in a design offers all of the benefits of an ARM design. These include principally:

1. The ability to move to your own custom ASIC if your product succeeds and the volumes grow. You can license the ARM core directly and create your own part without needing to re-write all of your software.
2. The rich family of available ARM and C software that is available on the WEB and can easily be ported to the ARM environment.

Packaging

Clarity 4 is a 0.25 micron design which is offered in three different configurations:

Clarity 4.1 is a 160 pin PQFP part, with 8 bit input and no external LCD support.

Clarity 4.2 is a 208 pin PQFP part with 12 bit input and support for an LCD.
Clarity 4.3 offers the functionality of Clarity 4.2 in a flex BGA package.

All the Clarity designs are manufactured for Sound Vision by Hynix Semiconductor in South Korea.

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The ASIC at a glance

ARM 7 TDMI, Interrupt and Memory Controllers

The ARM7TDMI is a 32 bit RISC (Reduced Instruction Set) processor that operates at 72MHz. It includes both a 32 bit and a 16 bit (Thumb Extension) instruction set. Attached to the processor is an 8Kbyte, single cycle, Cache for both instructions and data. The Interrupt Controller provides real time interrupts that indicate various events including DMA and I/O completion. The Memory Controller arbitrates all memory accesses between the external memory bus which is typically attached to a combination of SDRAM, NVRAM or ROM storage, and a set of internal DMA controllers and the Cache. Key to the Memory Controller is its ability to use burst accesses for all memory operations in order to sustain a maximum memory bandwidth of 72Mbytes per second.

DMA Controllers and FIFOs



All of the internal high speed peripherals attach to the memory controller through a combination of a DMA controller and a small 8 to 32 word FIFO. These FIFOs provide for the ability to burst data transfers into or out of memory, thus maintaining optimum performance.

USB and RS-232 (UART)

External interface to a host computer is typically obtained through either the USB Slave or UART interface. The USB interface includes a 16kbyte buffer memory that holds packets that are in the process of transmission between the systems. Data correction and retransmission is completely controlled within the USB interface.

The UART has an adjustable baud rate that can be set by the ARM processor up to 115kbaud. It attaches to the peripheral bus and provides an interrupt on various events. An external device is required to achieve the voltage levels associated with the RS-232 specification.

NTSC/PAL Output

The NTSC/PAL output generator includes a D/A converter and therefore produces an analog (base-band) signal that is compatible with the "video" input of most televisions. The ARM processor can set the interface, through software, to a number of different standards including NTSC, PAL B, M, N and CN.

An independent PLL (Phased Locked Loop) which is locked to the main oscillator creates the oscillator standard for these transmission modes. A 6 MHz crystal is used to derive the 72 MHz system clock, and then the 27 MHz required for the NTSC/PAL core is created internally.

Digital LCD

Other image display types are supported that accept digital raster data that is either color or monochrome. For example, these can include a small LCD or micro-display. Resolution and scan rates can be set under software control.

I²C Bus

An I²C Bus controller is included. It is typically attached to a "time of day" clock device, a status LCD driver or an external micro controller that can be used to extend the peripheral controls to additional buttons and display types.

Button Scanning

The button scan and sense logic supports up to 24 inputs using a set of 3 external 8:1 multiplexers. Button scanning and de-bouncing is done automatically without processor intervention.

Audio

The CODEC interface provides the timing and control necessary to perform proper handshaking with the Texas Instruments TLV320AC family of Voice-Band Audio Processors. It supports transmission and reception of serial data, generation of the associated frame sync pulses, along with a reference audio clock. The frame sync and master clock rates are selectable to support use with the 320AC36 and 320AC40 devices.

General Purpose I/O

There are eight groups of general purpose I/O (GPIO) signals, GPIOA – GPIOH; each group is multiplexed with other functions. An enable bit for each GPIO group selects between GPIO and the pre-defined functions.

Compact Flash and Smart Memory Interface

Software interfaces are offered to attach virtually any type of removable media including: CF, MMC, MS, SD, and SM. Of these, CF and SM are accelerated with custom hardware support.

Memory Interface

Clarity 4 can be connected to various external memory types including 100MHz SDRAM varying in size from 2Mbytes to 64Mbytes, and NVRAM or ROM ranging from 1Mbyte to 4Mbytes.

Acquisition Engine/Sensor Interface

The Sensor Interface includes a 12 bit digital port that is attached to an external A/D converter (sometimes included within a CMOS sensor). The interface contains several counters that can be either internally or externally synchronized to horizontal and vertical clocks. Therefore, it can easily be attached to a wide variety of CMOS and CCD sensors with their related interface components.

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